PRODUCT BRIEF

Alpha 21164 Microprocessor

The 21164 Alpha microprocessor (referred to as the 21164) is a high-performance implementation designed for Windows NT desktop PCs and workstations. The 21164 has a superscalar design capable of issuing four instructions every clock cycle. The integration of an instruction cache, data cache, and second-level cache provides unrivaled microprocessor performance. The 21164 uses a high-performance interface to access main memory, data buses, and an optional board-level cache.

Benefits

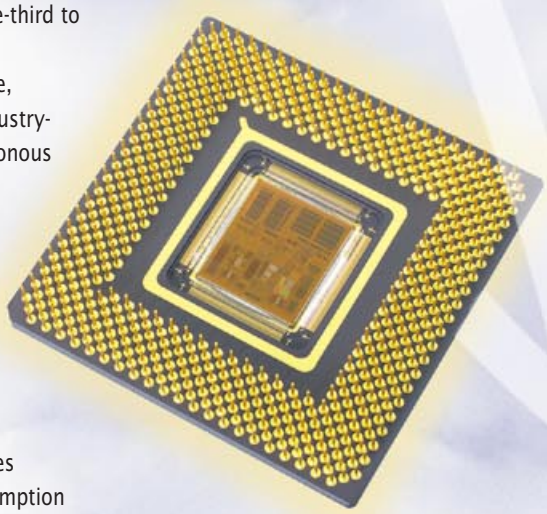
- Designed for the future using the 64-Bit Alpha architecture
- Increased engineering and business productivity
- Newest member of the award-winning 21164 family
- Highest performance Windows NT systems
- ATX motherboard turnkey OEM solution is available for quick time to market
- 100% Windows Compatible
- Thousands of native applications
  - High performance translation technology for x86 application
- Host-based DVD playback
- Designed to meet the needs of the computer industry
- Standard cooling

Applications

- Supports Windows NT
  - The first Windows NT 64-Bit platform
  - Runs non-native Windows NT applications using the DIGITAL FX!32 binary translator
- Supports DIGITAL UNIX
  - The first 64-Bit UNIX operating system
- Linux

Description

- Fully pipelined 64-Bit advanced RISC (reduced instruction set computing) architecture
- Best-in-class performance
  - 533HMz: 16.1 SPECint95, 22.5 SPECfp95
  - 600MHz: 18.0 SPECint95, 27.0 SPECfp95
  - 667MHz: 20.8 SPECint95, 32.4 SPECfp95 (estimated)
- Superscalar (4-way instruction issue)
- 0.35um CMOS technology
- Onchip, 8KB, direct-mapped L1 instruction cache
- Onchip, 8KB, direct-mapped, write-through L1 data cache
- Onchip, 96KB, 3-way, set-associative, write-back L2 unified instruction and data cache
- Memory-management unit
- Flexible high-performance interface
  - 128bit memory data path
  - 3.3-V I/O
- Selectable parity protection or error correction code (ECC) on data
  - Programmable system interface; one-third to one-fifteenth of clock speed
  - Control for optional offchip L3 cache, with multiple timing options for industry-standard synchronous and a synchronous SRAMs
- Serial ROM interface for initialization
- Chip- and module-level test supports JTAG (IEEE 1149.1)
- 499-pin ceramic interstitial pin grid array (IPGA) package
- Enhancements:
  - Support for byte and word data types
  - 2.0-V core for reduced power consumption

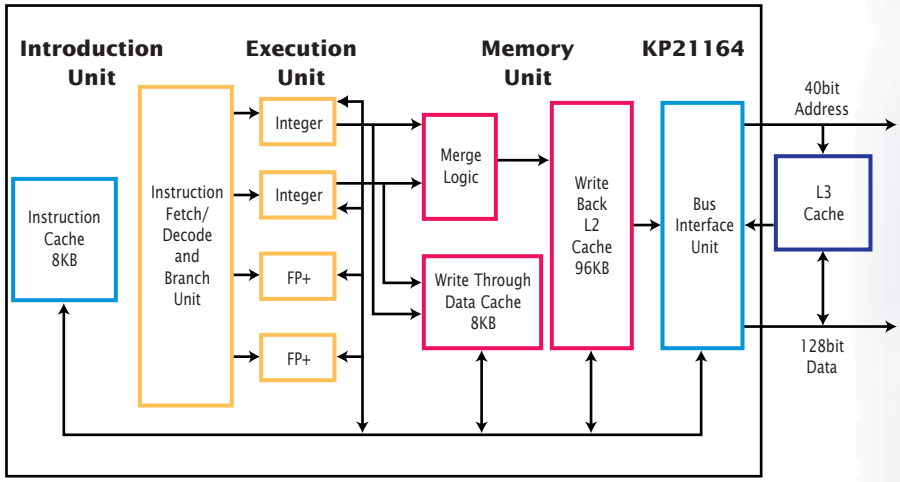


January, 1999

21164 Microarchitecture

The 21164 consists of five independent functional units: the instruction fetch, decode, and branch unit; the integer execution unit; the memory-management unit; the cache control and bus interface unit; and the floating-point unit. There are three on-chip caches: the instruction cache, the data cache, and the second-level cache.

21164 Functional Block Diagram



128bit Internal Data Bus

21164 Thermal Management

The 21164 dissipates approximately 43W at 500MHz. Conventional forced air cooling methods are sufficient to remove heat and maintain the highest levels of reliability. The user may also define an application-specific heat sink.

Power Supply	VSS = 0.0V, Vdd = 3.3V±5% Vddi = 2.5V±0.1V
Operating Temperature	Ta = 50˚C maximum (122˚F) Tj = 85˚C maximum (185˚F)
Storage Temperature Range	-55˚ C to +125˚ C (-67˚ F to +257˚ F)
Package	499- pin CPGA
Availability	Now

For More Information

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